

FACT SHEET

NetRAM™ Family

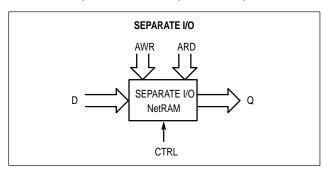
Fast SRAMs for the Communications Market

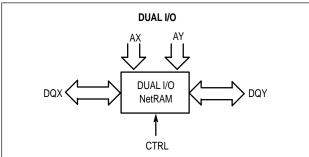
Motorola's NetRAMs are devices designed to best meet the optimal price and performance point for routers, switches, and dual-port like applications. These devices enable data to flow quickly so Local Area Network (LAN) and Wide Area Network (WAN) devices can devote more of their resources to application performance.

GENERAL DESCRIPTION

NetRAMs are 1 Megabit static random access memory, organized as 32K x 36 and 64K x 18. They feature separate LVTTL input and output buffers and incorporate input and output registers on board with high speed SRAM.

The MCM69D536, MCM69D618, MCM69Q536, and MCM69Q618 feature two address ports and two data ports. Each address port controls its respective data port.





SUGGESTED APPLICATIONS

- ATM Switches
- Ethernet Switches
- Routers
- Cell/Frame Buffers
- SNA Switches
- · Shared Memory

Dual Address, Dual I/O Features MCM69D536, MCM69D618

- Single 3.3 V ± 5% Power Supply
- Fast Access Times: 8/10 ns Max
- Single Clock Operation
- Address, Data Input, E1, E2, PTX, PTY, WX, WY Registers on Chip
- 66 MHz Maximum Clock Cycle Time
- Self Timed Write
- Two Bi-Directional Data Buses
- · Pass-Through Feature
- Asynchronous Output Enable (GX, GY)
- 176 Pin TQFP Package for the x 36
- 100 Pin TQFP Package for the x 18

Dual Address, Separate I/O Features MCM69Q536, MCM69Q618

- Single 3.3 V ± 5% Power Supply
- Fast Access Times: 8/10 ns Max
- Single Clock Operation
- Address, Data Input, E1, E2, PT, W Registers on Chip
- 66 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Data Output Pins
- Pass–Through Feature
- Asynchronous Output Enable (G)
- 176 Pin TQFP Package for the x 36
- 100 Pin TQFP Package for the x 18

Single Address, Separate I/O Features MCM69Q537, MCM69Q619

- Single 3.3 V ± 5% Power Supply
- Fast Access Times: 5 ns Max
- Single Clock Operation
- Address, Data Input, E1, E2, PT, W Registers on Chip
- 150 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Data Output Pins
- Pass-Through Feature
- Asynchronous Output Enable (G)
- 176 Pin TQFP Package for the x 36
- 100 Pin TQFP Package for the x 18

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REV 1 9/4/96

APPLICATION EXAMPLES

Dual Port Like Applications

A family of Fast SRAMs has been developed to support dual—port applications at a much lower price. These memories offer separate addresses with dual inputs and outputs allowing designers to simulate the functionality of a dual—port. This allows for statistical gathering on one side and performance management on the other. Dual input/output devices provide the optimal performance in applications in which one requires the ability to access different locations at the same time, effectively doubling the speed of data transfer.

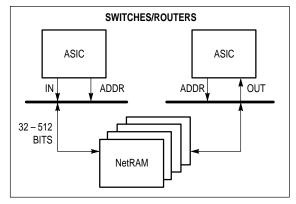
Fabric Switch Applications

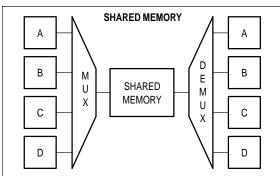
Separate I/O, dual address allows reads and writes to occur in the same cycle. By splitting the bus and doubling the bandwidth, there is greater utilization of the shared memory.

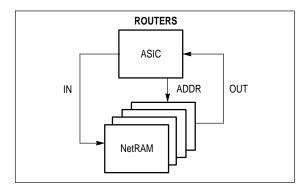
Cells from any connection can be put into the shared memory based on the depth of the memory. Cells can be partitioned based on priorities and quality of service.

Router Table Applications

Single address, separate I/O devices add value to router table designs by allowing data to be both read into and written out of the memory simultaneously. This decreases the time required for data transmission and increases the bandwidth of the bus. Devices also well suited for this application include the 128K x 9 MCM67Q709, the 256K x 4 MCM67Q804, the 512K x 9 MCM67Q909, as well as the 32K x 36 and 64K x 18, MCM69Q536 and MCM69Q618.







For additional information call 512–933–SRAM, or your local Motorola sales representative. FAX (512) 933–6809

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